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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/619,912	07/15/2003	Kevin Somervill	200208712-1	7161

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EXAMINER	
BARAN, MARY C	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,912	SOMERVILL ET AL.	
	Examiner	Art Unit	
	Mary Kate B Baran	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: on page 4 line 21, "that" should be – than –.

Appropriate correction is required.

Drawings

2. This application has been filed with informal drawings, which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 8-10, 15-17, 19-21 and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Nejedlo et al. (U.S. PG-Pub No. 2004/0117709) (hereinafter Nejedlo).

Referring to claim 1, Nejedlo teaches a method of testing an electronic device (see Nejedlo, page 2 [0021]), said method comprising: transferring a test pattern between a first data controller coupled to a first data interface and a second data controller coupled to a second data interface via an element coupling said first and second data interfaces (see Nejedlo, page 3 [0028]); receiving said test pattern (see Nejedlo, page 4 [0033]); and examining said test pattern (see Nejedlo, page 4 [0038]).

Referring to claim 2, Nejedlo teaches transferring said test pattern between said first data controller and a third data controller coupled to a third data interface via an element coupled between said first data interface and said third data interface (see Nejedlo, page 3 [0028]).

Referring to claim 3, Nejedlo teaches that said test pattern tests electrical connectivity over between said first data controller and said second data controller (see Nejedlo, page 1 [0015]).

Referring to claim 6, Nejedlo teaches transferring said test pattern over data interfaces comprising, a PCI interface (see Nejedlo, page 2 [0019]) and a memory interface (see Nejedlo, page 2 [0017]).

Referring to claim 8, Nejedlo teaches establishing a drive mode for said first data controller (see Nejedlo, page 4 [0033]); and establishing a receive mode for said second data controller (see Nejedlo, page [0034]).

Referring to claim 9, Nejedlo teaches an apparatus for testing an electronic device, said apparatus comprising: a first element that is operable to be inserted into a first data interface (see Nejedlo, Figure 1A) coupled to a first data path of the electronic device (see Nejedlo, page 2-3 [0023]); a second element that is operable to be inserted into a second data interface coupled to a second data path of the electronic device (see Nejedlo, Figure 1A), wherein said first sand second data interfaces are not typically connected during operation of the electronic devices (see Nejedlo, page 2-3 [0023]); and a third element coupled between said first element and said second element to allow an electrical coupling of the first data interface to the second data interface, wherein said electrical coupling allows the formation of a test data path including the first and second data paths (see Nejedlo, Figure 2).

Referring to claim 10, Nejedlo teaches a fourth element that is operable to be inserted into a third data interface coupled to a third data path of the electronic device (see Nejedlo, Figure 1A); and wherein said third element is further coupled between said first element and said fourth element to allow an electrical coupling of the first data interface to the third data interface, wherein said electrical coupling of the first data

interface to the third data interface allows the formation of a test data path including the first and third data paths (see Nejedlo, pages 1-2 [0016]).

Referring to claim 15, Nejedlo teaches that said second element is adapted to be inserted into a memory slot (see Nejedlo, pages 2-3 [0023]).

Referring to claim 16, Nejedlo teaches that said second element is adapted to be inserted into a disk drive slot (see Nejedlo, pages 1-2 [0016]).

Referring to claim 17, Nejedlo teaches that said electrical coupling further allows an electrical connectivity test (see Nejedlo, page 1 [0015]).

Referring to claim 19, Nejedlo teaches a computer readable medium having stored therein instructions that when executed on a processor implement a method of testing an electronic device (see Nejedlo, page 2 [0021]), said method comprising: issuing a command to a first data controller to transfer a test pattern from said first data controller to a first data interface coupled thereto (see Nejedlo, page 3 [0028]); and issuing a command to a second data controller to receive said test pattern from a second data interface that is electrically coupled between said first data interface and said second data controller (see Nejedlo, page 4 [0037]); and receiving said test pattern (see Nejedlo, page 4 [0037]).

Referring to claim 20, Nejedlo teaches issuing a command to a third data controller to receive said test pattern from a third data interface that is electrically coupled between said third data controller and said first data interface (see Nejedlo, page 3 [0028]).

Referring to claim 21, Nejedlo teaches that said method further comprises determining that a data path exists from said first data controller to said second data controller through a path including said first and second data interfaces (see Nejedlo, page 3 [0028]).

Referring to claim 23, Nejedlo teaches that said method further comprises performing an electrical connectivity test of a data path comprising said first data interface and said second data interface (see Nejedlo, page 1 [0015]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 5, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nejedlo et al. (U.S. PG-Pub No. 2004/0117709) (hereinafter Nejedlo) in view of Marchevsky (U.S. Patent No. 6,572,384).

Referring to claims 4 and 5, Nejedlo teaches all the features of the claimed invention except transferring said test pattern over data interfaces having the same or different form factors.

Marchevsky teaches transferring said test pattern over data interfaces having the same or different form factors (see Marchevsky, column 6 lines 33-47).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Nejedlo to include the teachings of Marchevsky because interfaces with multiple and varied form factors are common in various devices under test and would have allowed the skilled artisan to use the testing method on various electronic devices.

Referring to claims 11 and 12, Nejedlo teaches all the features of the claimed invention except that said first element and said second element are adapted to be inserted to data interfaces having the same or different form factors.

Marchevsky teaches that said first element and said second element are adapted to be inserted to data interfaces having the same or different form factors (see Marchevsky, column 6 lines 33-47).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Nejedlo to include the teachings of Marchevsky because interfaces with multiple and varied form factors are common in various devices under test and would have allowed the skilled artisan to use the testing method on various electronic devices.

5. Claims 7, 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nejedlo et al. (U.S. PG-Pub No. 2004/0117709) (hereinafter Nejedlo) in view of Rajski et al. (U.S. Patent No. 5,991,898) (hereinafter Rajski).

Referring to claim 7, Nejedlo teaches all the features of the claimed invention except that said first and second data controllers are both tested using a single scan chain.

Rajski teaches that said first and second data controllers are both tested using a single scan chain (see Rajski, column 11 lines 13-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Nejedlo to include the teachings of Rajski because using a single scan chain would have allowed the skilled artisan to generate the test pattern from the pre-computed compressed pattern (see Rajski, column 11 lines 31-35).

Referring to claim 18, Nejedlo teaches all the features of the claimed invention except that said electrical coupling further allows multiple data controllers to be tested using a single scan chain.

Rajski teaches that said electrical coupling further allows multiple data controllers to be tested using a single scan chain (see Rajski, column 11 lines 13-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Nejedlo to include the teachings of Rajski because using a

single scan chain would have allowed the skilled artisan to generate the test pattern from the pre-computed compressed pattern (see Rajski, column 11 lines 31-35).

Referring to claim 22, Nejedlo teaches all the features of the claimed invention except that said method further comprises testing a plurality of data controllers using a single scan chain.

Rajski teaches that said method further comprises testing a plurality of data controllers using a single scan chain (see Rajski, column 11 lines 13-15).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Nejedlo to include the teachings of Rajski because using a single scan chain would have allowed the skilled artisan to generate the test pattern from the pre-computed compressed pattern (see Rajski, column 11 lines 31-35).

6. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nejedlo et al. (U.S. PG-Pub No. 2004/0117709) (hereinafter Nejedlo) in view of Allen et al. (U.S. Patent No. 6,237,048) (hereinafter Allen).

Referring to claims 13 and 14, Nejedlo teaches all the features of the claimed invention except that said first element comprises a plug-in jumper card adapted to be inserted into a PCI card slot.

Allen teaches that said first element comprises a plug-in jumper card adapted to be inserted into a PCI card slot (see Allen, column 3 lines 56-63).

It would have been obvious at the time the invention was made to one of ordinary skill in the art to modify Nejedlo to include the teachings of Allen because using plug-in jumper cards would have allowed the skilled artisan to enable, disable or select the various signal lines connecting the card to the interface (see Allen, column 3 liens 9-14)

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(a) Moberly teaches scan path test support.

(b) Tanner teaches a method and system for testing interconnected integrated circuits.

(c) Basto et al. teach a graphical user interface for testability operation.

(d) Adachi et al. teach a manufacturing method of semiconductor integrated circuit device.

(e) Angelotti et al. teach testing system interconnections using dynamic configuration and test generation.

(f) Noguchi teaches a semiconductor integrated circuit and recording medium.

(g) Pratt et al. teach a removable storage media drive feature enabling self test without presence of removable media.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary Kate B. Baran whose telephone number is (571)

272-2211. The examiner can normally be reached on Monday - Friday from 9:00 am to 6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (571) 272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

09 February 2004

MARC S. HOFF
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